EE 230
Lecture 37

Data Converters

ADC and DAC Architectures

Study Abroad Opportunities

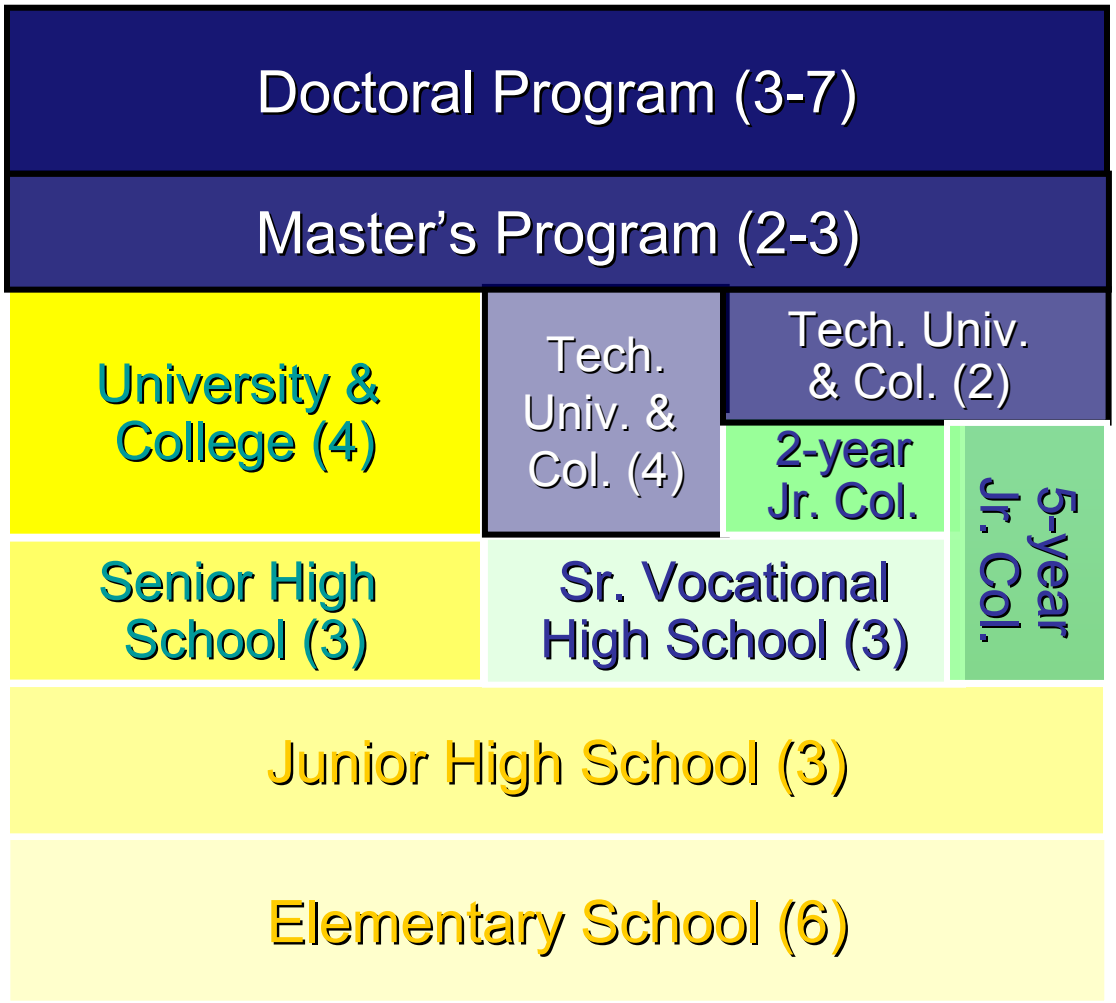
The increasing role Asia is playing in both the engineering field and the world's economy is unlike anything we have seen in many decades

All indicators suggest that this role will become even more significant in the future

Both opportunities and expectations in the field will invariable show increased alignment with business and engineering in a global economy

Understanding the culture and the environment of engineers working in Asia will offer substantial benefits for many/most engineers in the short-term and will likely be expected of many/most engineers within a decade

Taiwan's Education System



- Have identified two schools in Taiwan that will offer selected courses to ISU students in English
- Courses pre-approved so that progress towards graduation is not delayed
- Revenue neutral exchange (often costs less than spending the time in Ames)
- Internship opportunity often provided

Tatung University

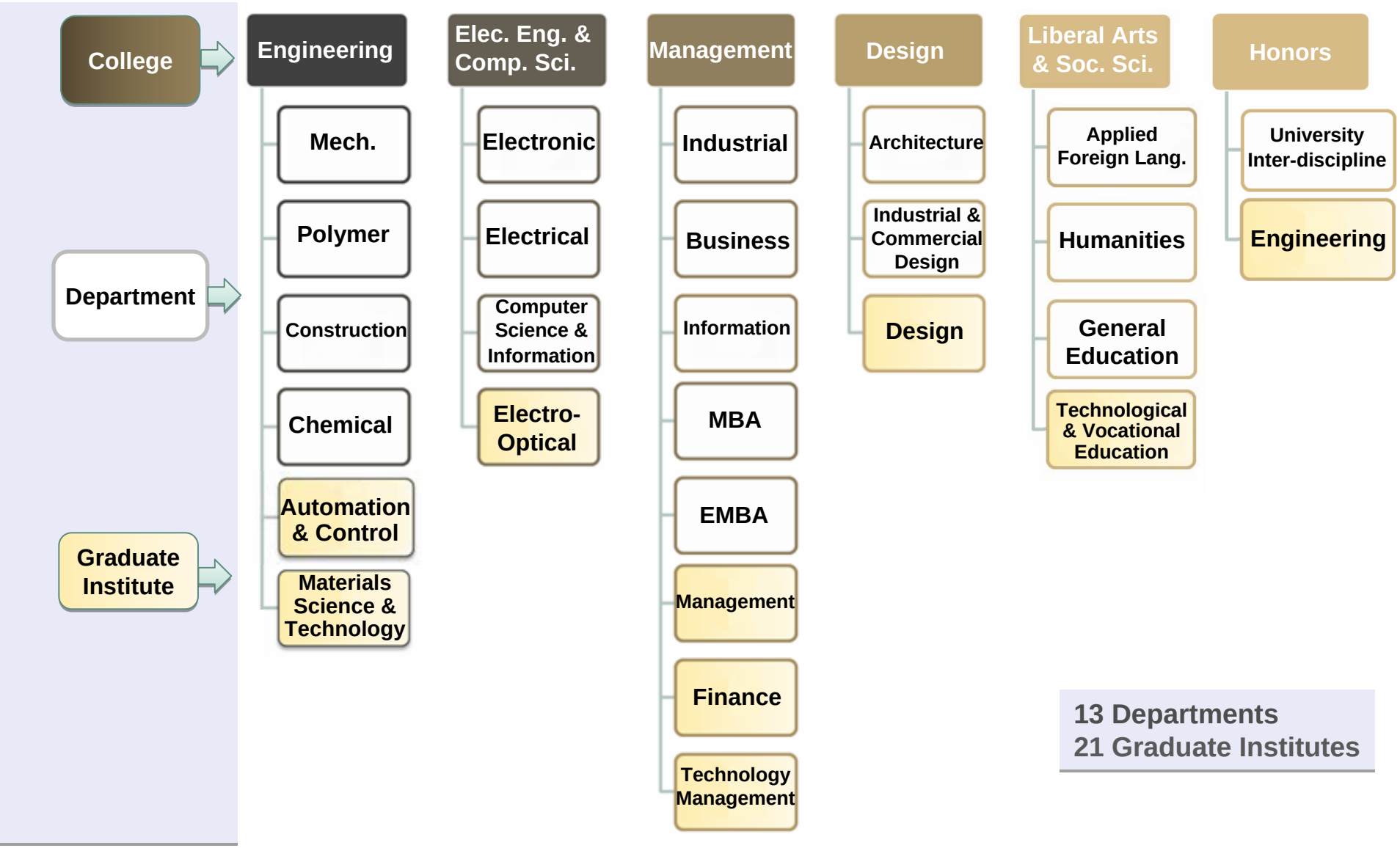
Welcome


尚志教育研究館

TAIWAN TECH

National Taiwan University of Science and Technology

Current Status / Academics



High-rise Building Earthquake-Resistant Beam Patent

Patent used in almost 86 buildings and in the Taipei 101 Skyscraper

HPC Patent

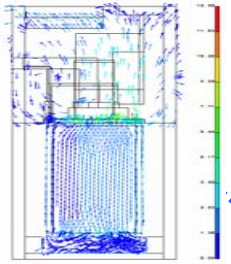
Used in Tuntex Sky Tower, Kao-hsiung

- Automation & Control Center
- Center for Intelligent Robots
- Center for the Study of Lottery & Commercial Gaming
- Communication & Electromagnetic Technology Center
- Construction Occupation Health & Safety Center
- Ecological & Hazard Mitigation Engineering Research Center
- Expensive Instrument Center
- Materials Science & Technology Center
- Nanotechnology Engineering Center
- Opto-Mechatronics Technology Center
- Power Electronics Technology Center
- Taiwan Information Security Center

Opto-Mechatronics Technology Center

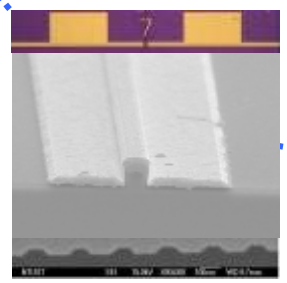
Opto-Mechatronics component design & manufacturing

Low db Plastic Optical Fiber



Disk Array heat transfer analysis

Opto-Mechatronics sub-system



Double-wave length laser light

Opto-Mechatronics system design & integration

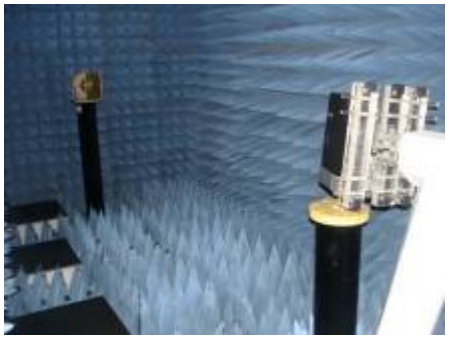
Micro-drill Laser inspection system

Communication and Electromagnetic Technology Center

Major Research Topics

- Miniature Chip Antennas
- Radio-Frequency Identification (RFID)
- Antennas and Wave Propagation for Wireless Communications
- RF, Microwave, and Millimeter Wave Circuits
- Communication Systems
- Integrated Circuit Designs
- Electromagnetic Interferences at Power and Radio Frequencies
- Electromagnetic Properties of Materials

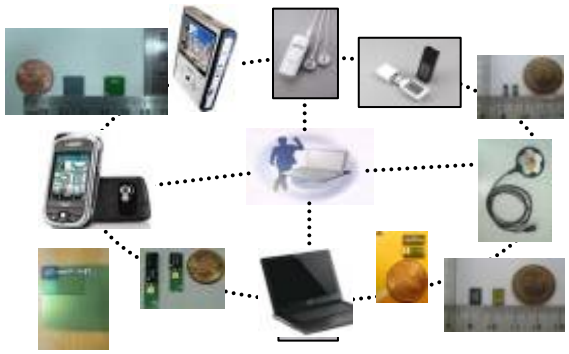
Multi-function Anechoic Chamber

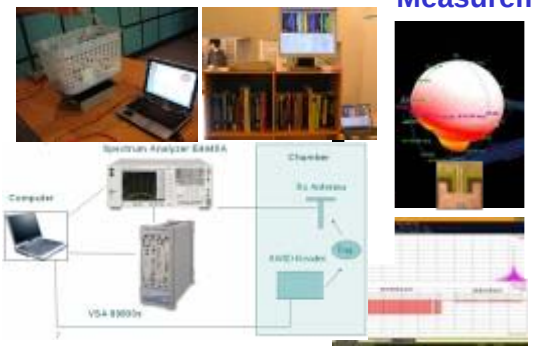


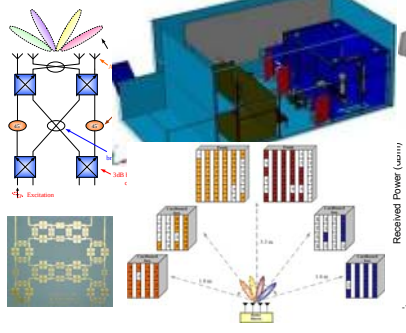
Far Field Measurement Anechoic Chamber

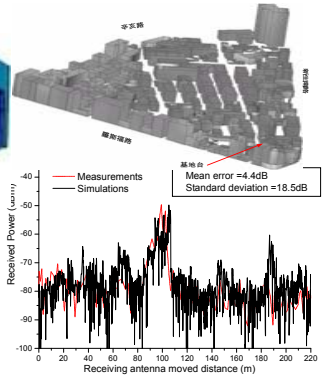
Planar/Cylindrical Near Field Measurement Chamber

EMC Semi-anechoic Chamber





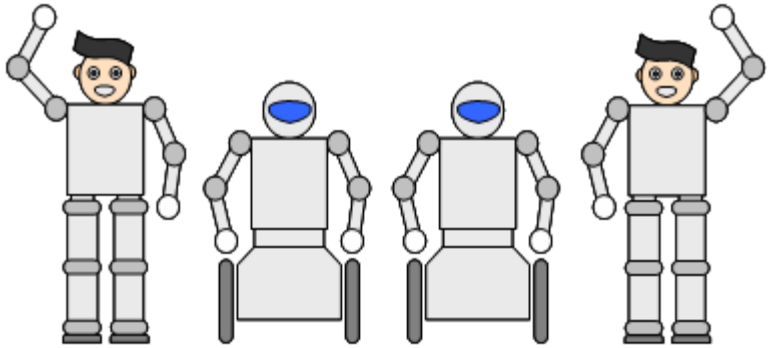


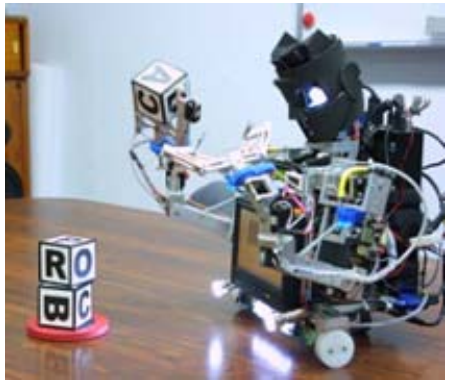


Center for Intelligent Robots

Robot Theater

Dancing, Singing, Imitation show
Drawing… etc.

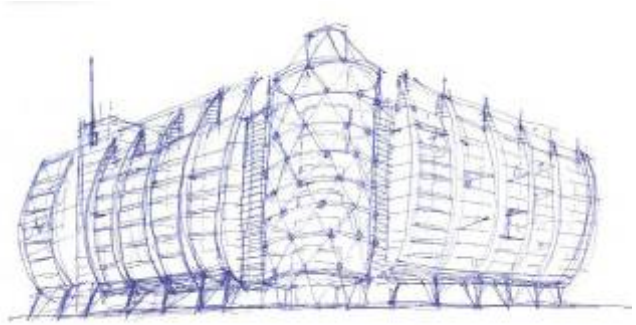


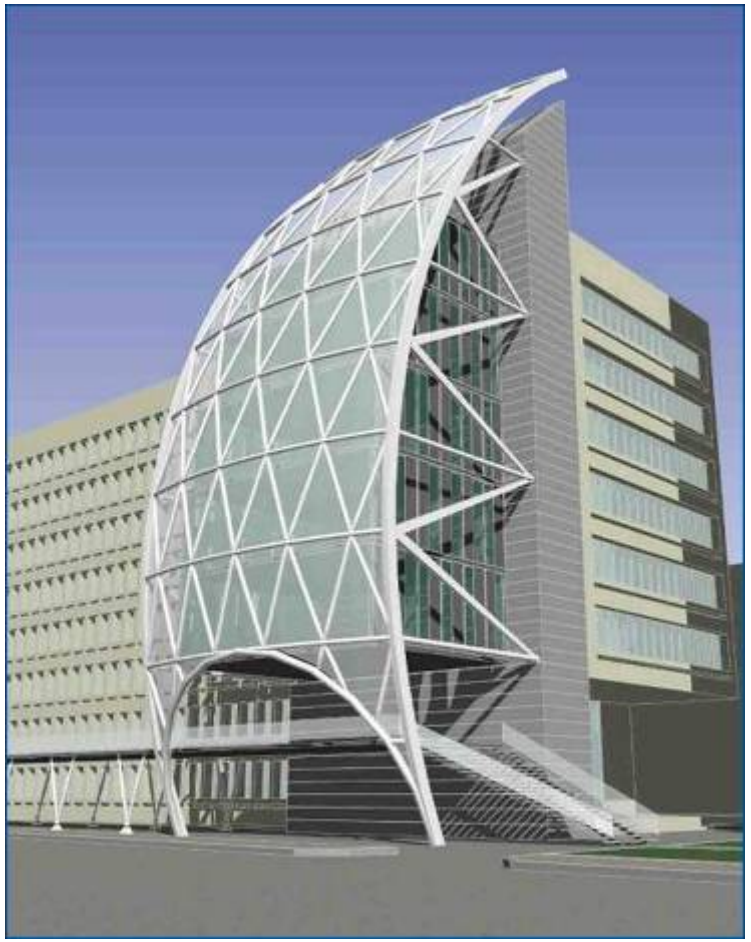


Intelligent Robot DOC-1 & DOC-2

Teach English Spelling
Solve Algebraic Problem
Play Gobang, Chess and Chinese Chess
Recognize Human Faces
Interpret Facial Expressions

- Building Energy Efficiency and Renewable Energy Center
- Building Structure and Hazard Mitigation Center
- Green Building Materials Center
- Intelligent Building Research Center
- New Generation Building Systems Center
- Steel Structure Engineering Center





International Partnerships

- ***U.S.*** Ohio State Univ., Univ. of California-Berkeley, Tulane Univ., Univ. of Kansas, Rochester Inst. of Technology, etc.
- ***Central America*** Univ. of San Carlos, etc.
- ***Europe*** Univ. of Leeds, ETH Zurich, EPF Lausanne, Ecole Speciale D'Architecture, Univ. Rene Descartes Paris, Czech Technical Univ./Prague, etc.
- ***Australia*** Queensland Univ. of Technology, etc.
- ***Asia*** Kanagawa Univ., Tokyo University, Moscow State Technical Univ., Moscow Aviation Inst., Institut Teknologi Sepuluh Nopember, Institut Teknologi Bandung, Univ. of Mongolia, Univ. of the Philippines

Study Abroad Opportunities in Asia

Programs exist with both Tatung University and National Taiwan University of Science and Technology – both are in Taipei

Both are good schools and both should provide a good study abroad opportunity

If interested in either program make the following contacts:

Tatung University

Prof. Morris Chang (ISU coordinator) or
Prof. Randy Geiger

National Taiwan University of Science and Technology

Prof. Randy Geiger (ISU coordinator)

Review from Last Time:

Engineering Issues for Using Data Converters

1. Inherent with Data Conversion Process

- Amplitude Quantization
- Time Quantization

(Present even with Ideal Data Converters)

2. Nonideal Components

- Uneven steps
- Offsets
- Gain errors
- Response Time
- Noise

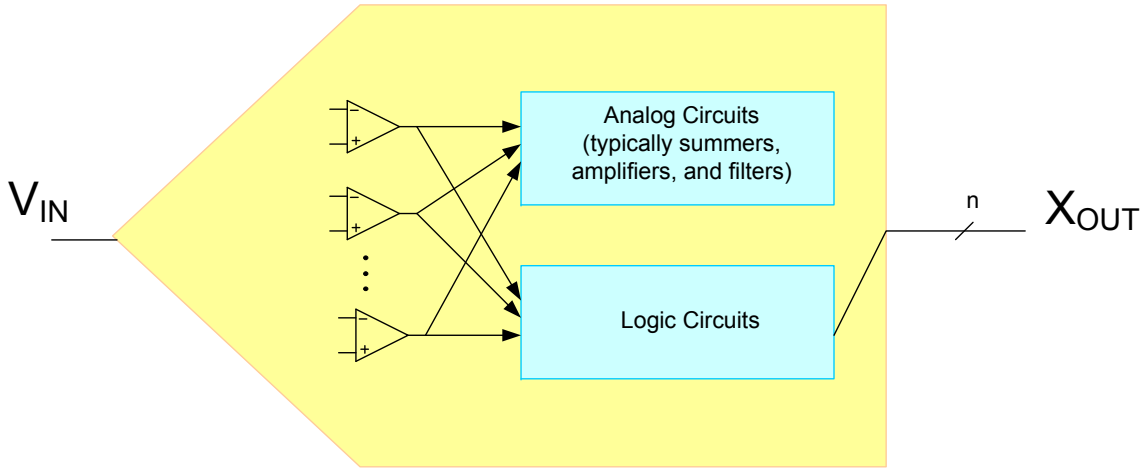
(Present to some degree in all physical Data Converters)

How do these issues ultimately impact performance ?

Review from Last Time:

ADC Architectures

Essentially all ADCs use one or more comparators to convert an analog signal to a digital signal. They typically include some other analog circuitry and some digital circuitry



Review from Last Time:

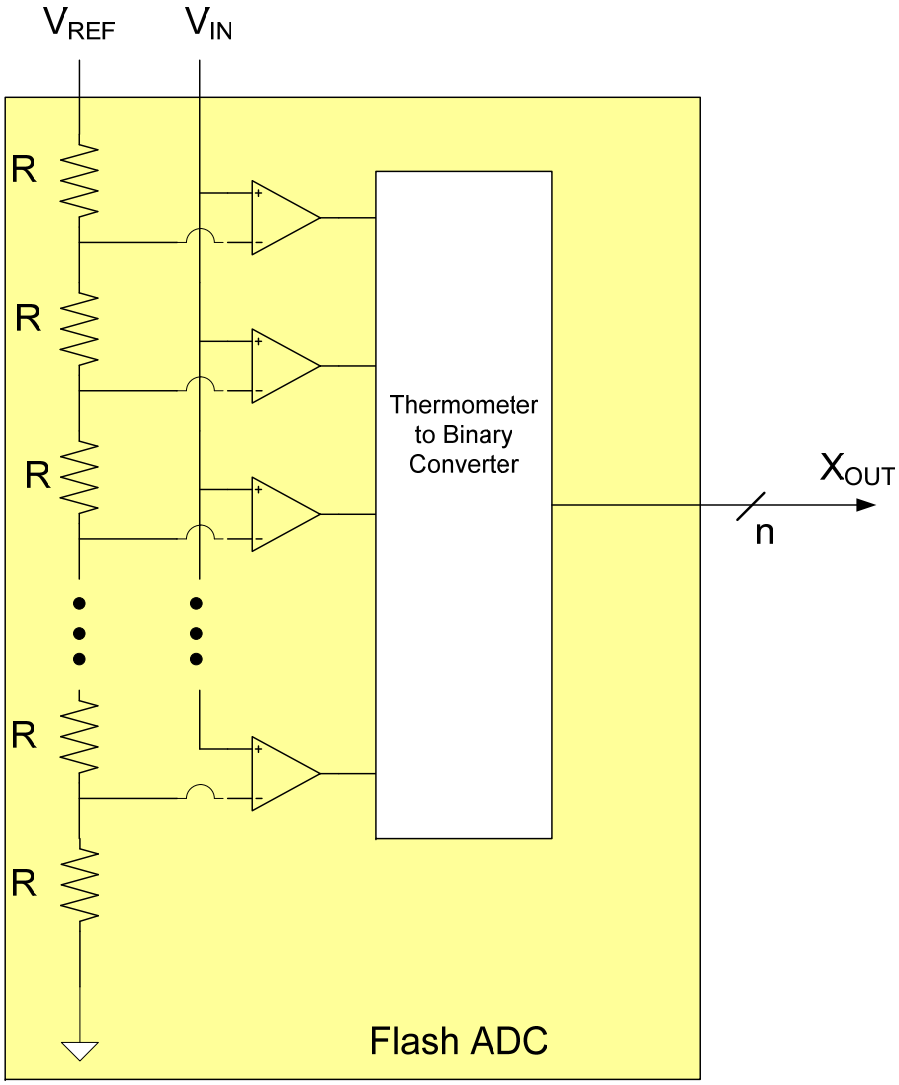
Types of ADCs

- Flash
- Pipelined
- Folded
- Serial
  - Single-slope
  - Dual-slope
- Interpolating
- Iterative (Algorithmic, Cyclic)
- Successive Approximation (SAR)
- Oversampled (Delta-Sigma)
- Charge Redistribution
- Several others

Review from Last Time:

Types of ADCs

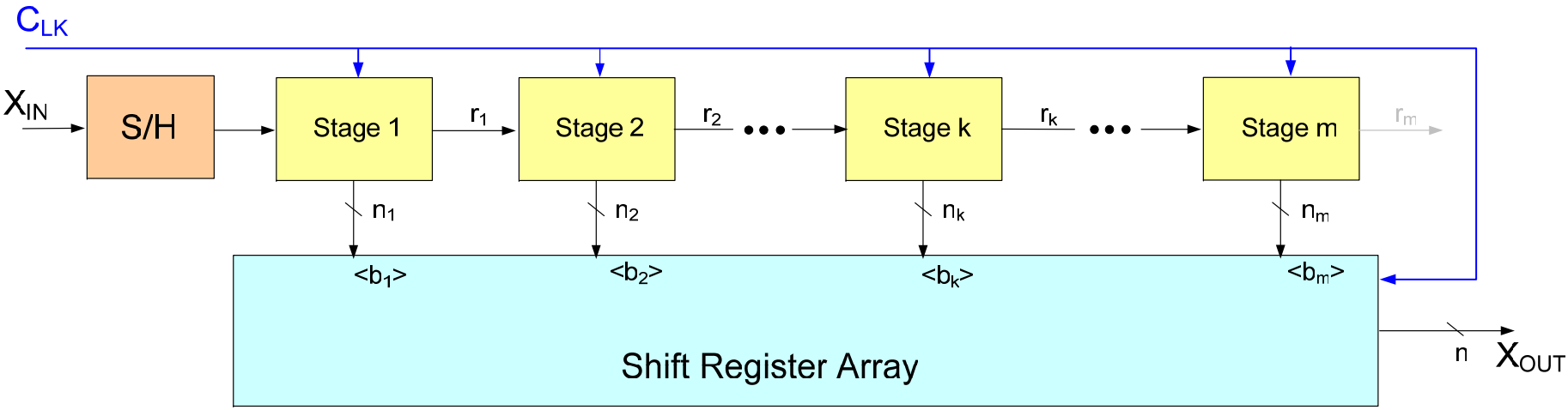
Flash ADC

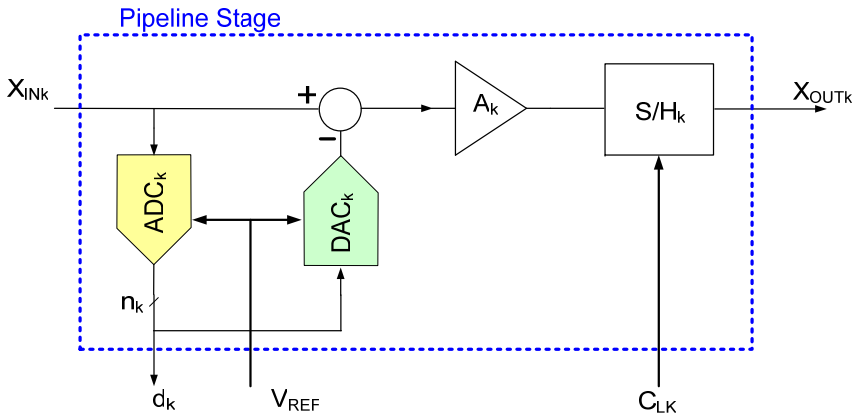


Review from Last Time:

Types of ADCs

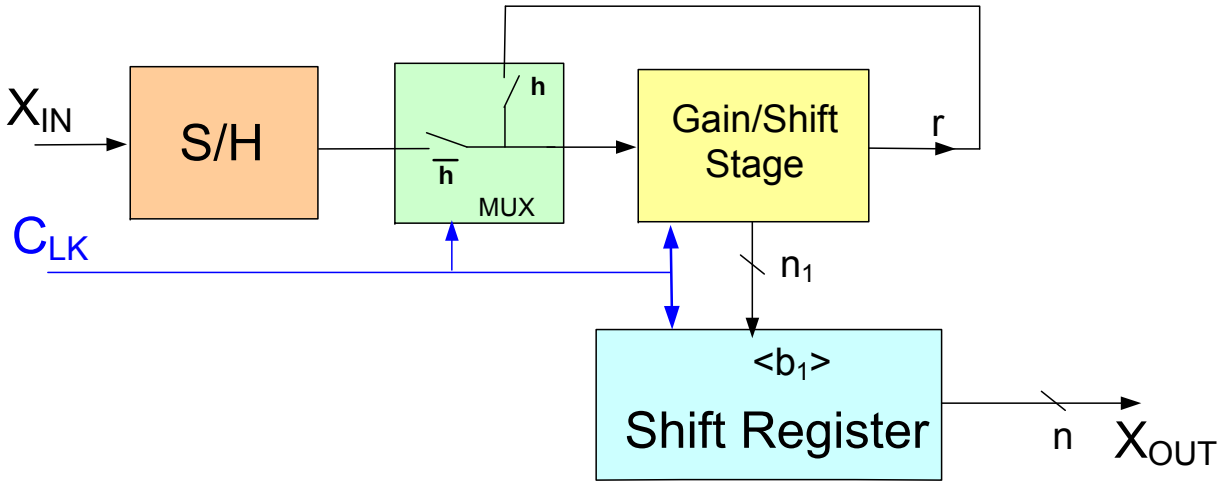
Pipelined ADC

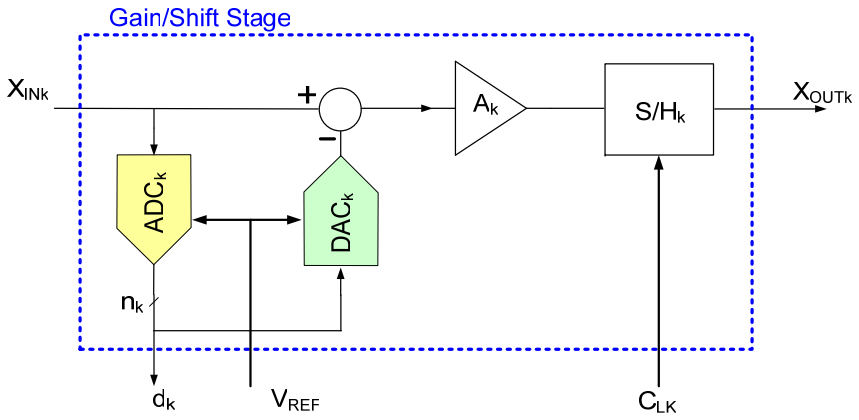




Types of ADCs

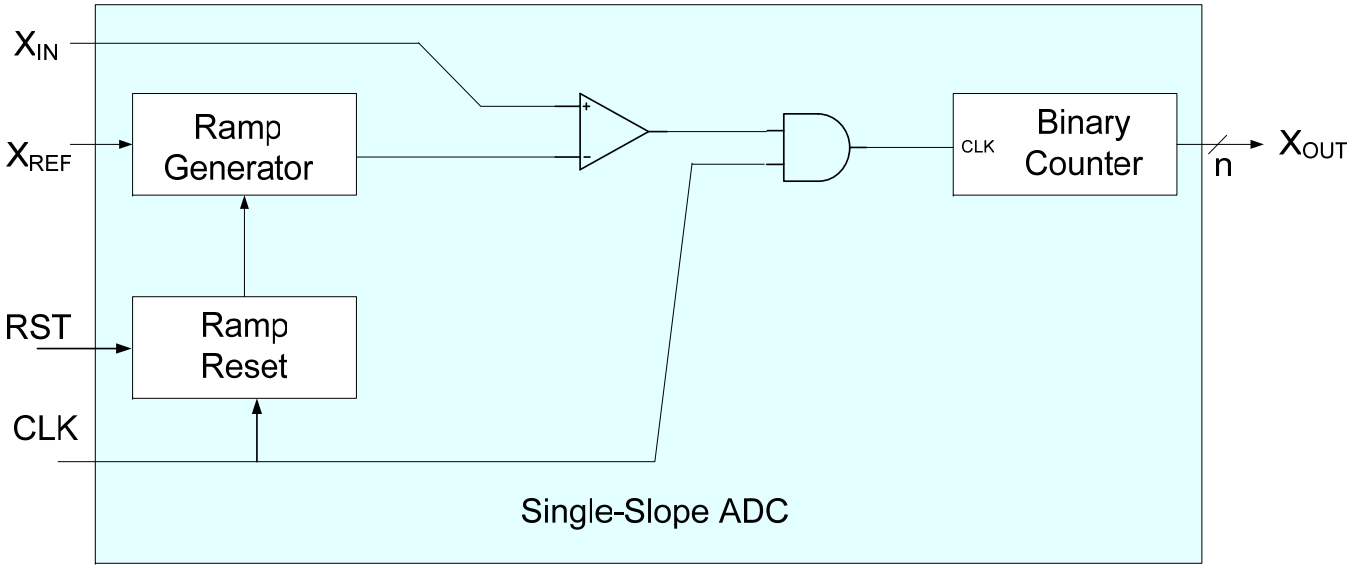
Cyclic ADC





Types of ADCs

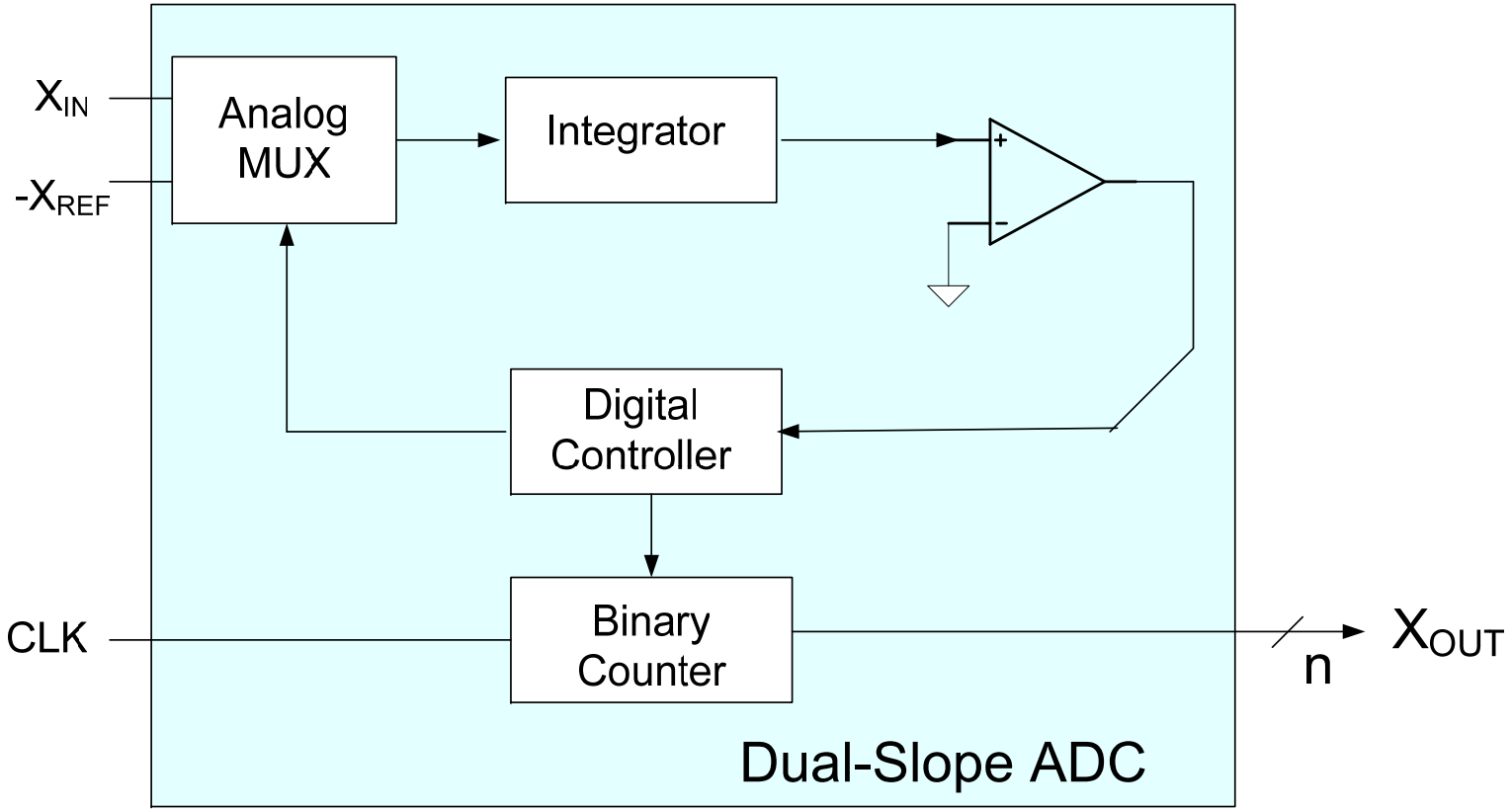
Single-Slope ADC



Counter counts up to <1 1 1 ,,, 1> when ramp reaches V_{REF}

Types of ADCs

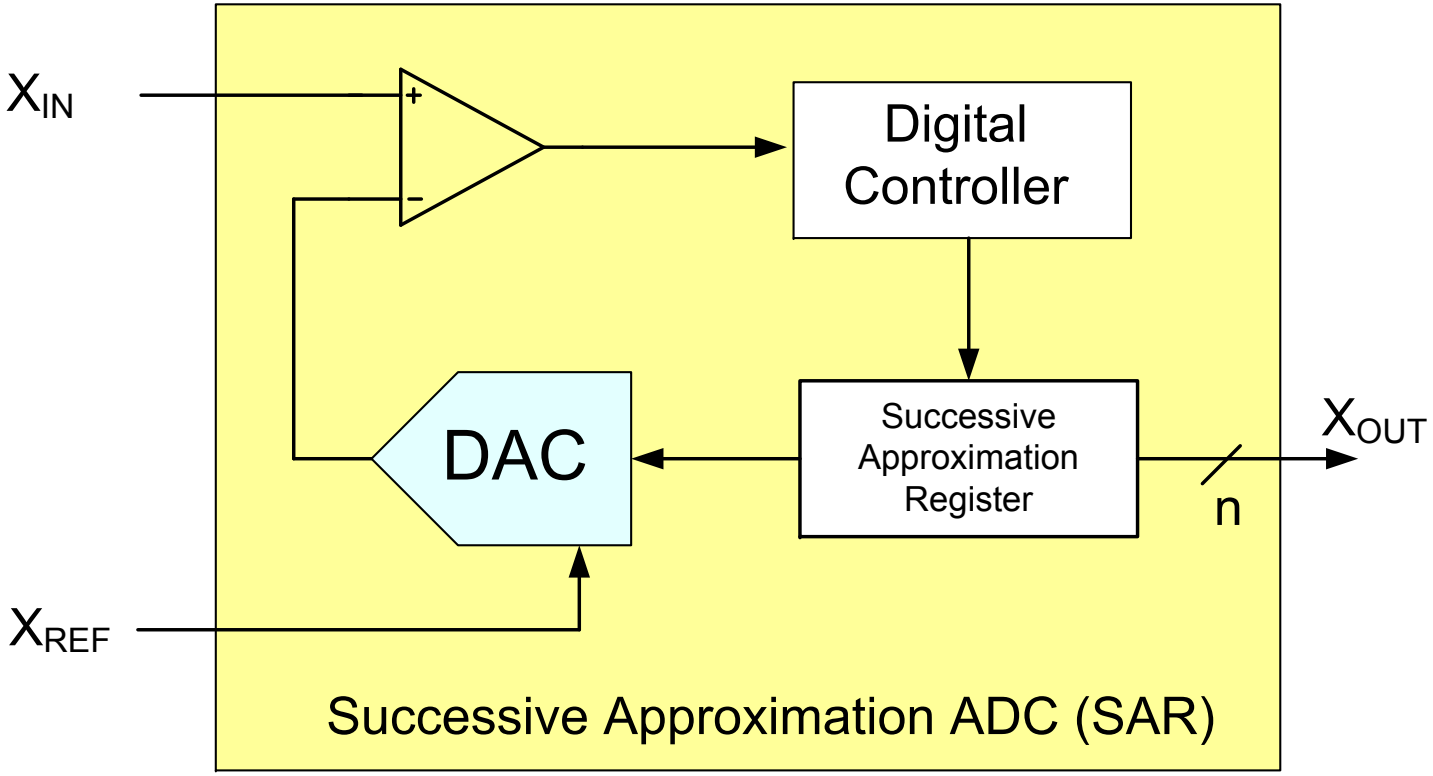
Dual-Slope ADC



Integrator ramps up from 0 for fixed time with X_{IN} as input
Integrator then ramps down with $-X_{REF}$ as input and counter stops when reaches 0

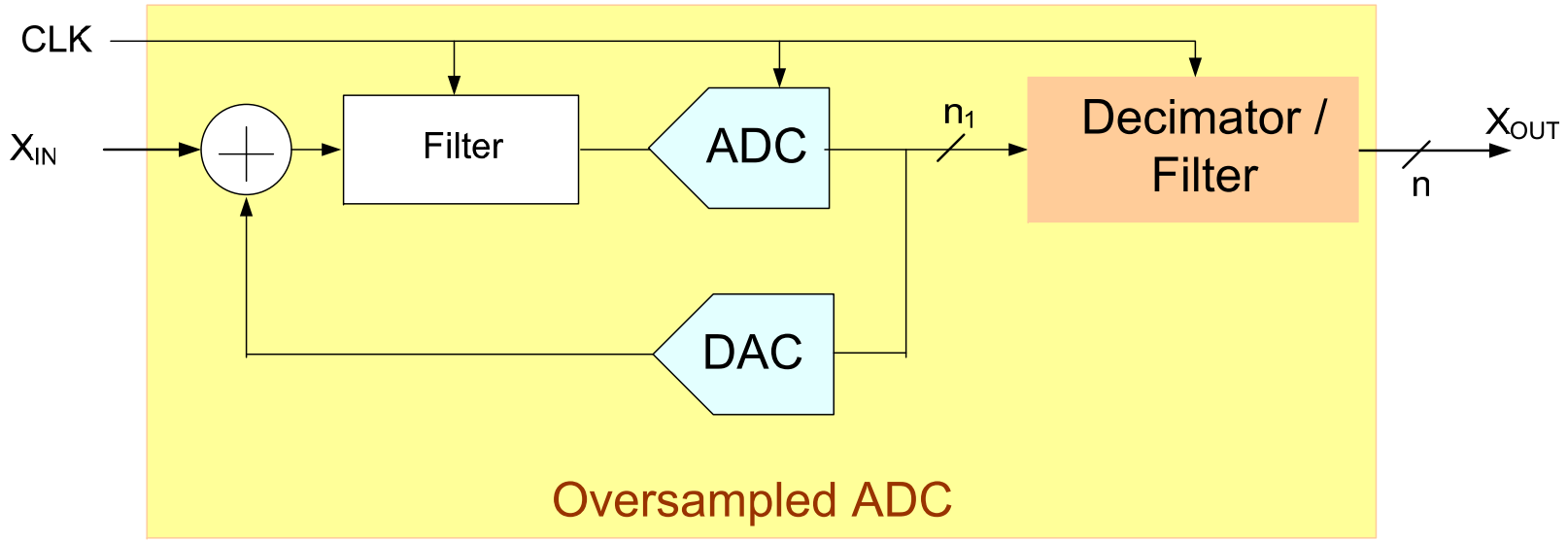
Types of ADCs

SAR ADC



Types of ADCs

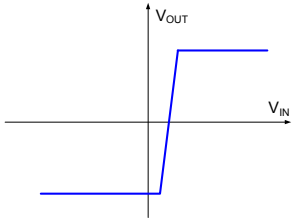
Over-sampled ADC (Delta-Sigma)



ADC is often simply a comparator
CLK is much higher in frequency than effective sampling rate (maybe 128:1)
Can obtain very high resolution but effective sampling rate is small

Metastability

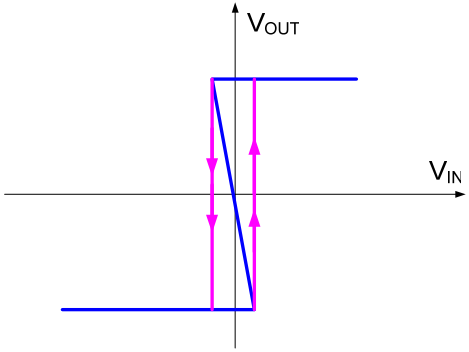
High-gain amplifier



for some input values, output may not be at a level that is predictably interpreted by subsequent logic circuits

this range can be very small if the gain is large enough

Bistable amplifier



Bistable amplifier will always make a decision

For any fixed finite time T, there is always a small nonzero probability that the decision will not be made in time T

This probability can be made very low through proper circuit design techniques but never made to be zero

Metastability

Metastability in ADCs caused by comparators

A comparator is said to be in a metastable state if the output of the comparator can not be interpreted by subsequent digital logic

For any finite time T, any comparator that has been "asked" to make a binary decision has a finite nonzero probability P that subsequent logic will not correctly interpret the output In the interval of length T

This probability can be made very low through proper circuit design techniques but never made to be zero

Metastability in ADCs caused by transient conditions in logic circuits

Due to asynchronous operation of the ADC

Can be eliminated by circuit modifications that make operation synchronous or by appropriate timing of asynshronous operation

Metastability

Flash ADC

Interpolating

Pipelined

Successive Approximation (SAR)

Iterative (Algorithmic, Cyclic)

Serial

Folded

Oversampled (Delta-Sigma)

Dual-slope

Charge Redistribution

Single-slope

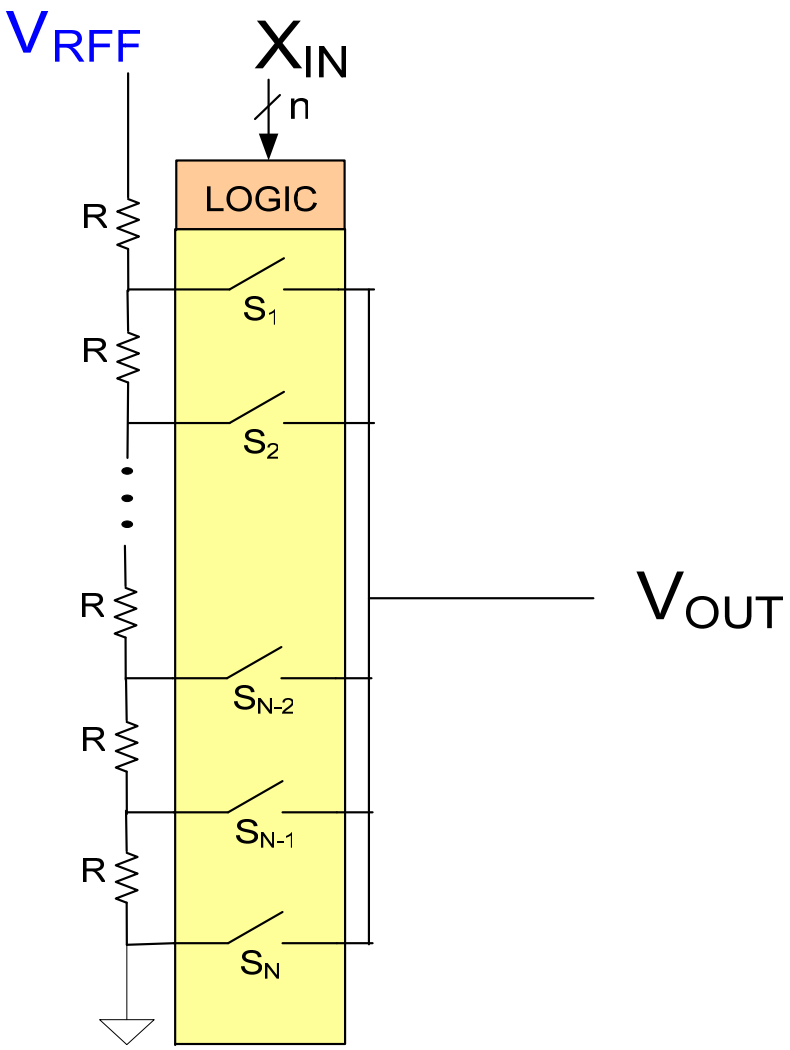
Metastability can never be eliminated in an ADC, its effects can just be reduced to a level that results in an acceptably low probability of causing an unacceptable outcome

Types of DACs

- Current steering
- R-String
- Ladder (R-2R)
- Parallel
- Pipelined
- Subranging
- Charge Redistribution
- Algorithmic
- Serial
- Subranging
- Oversampled (Delta-Sigma)
- Several others

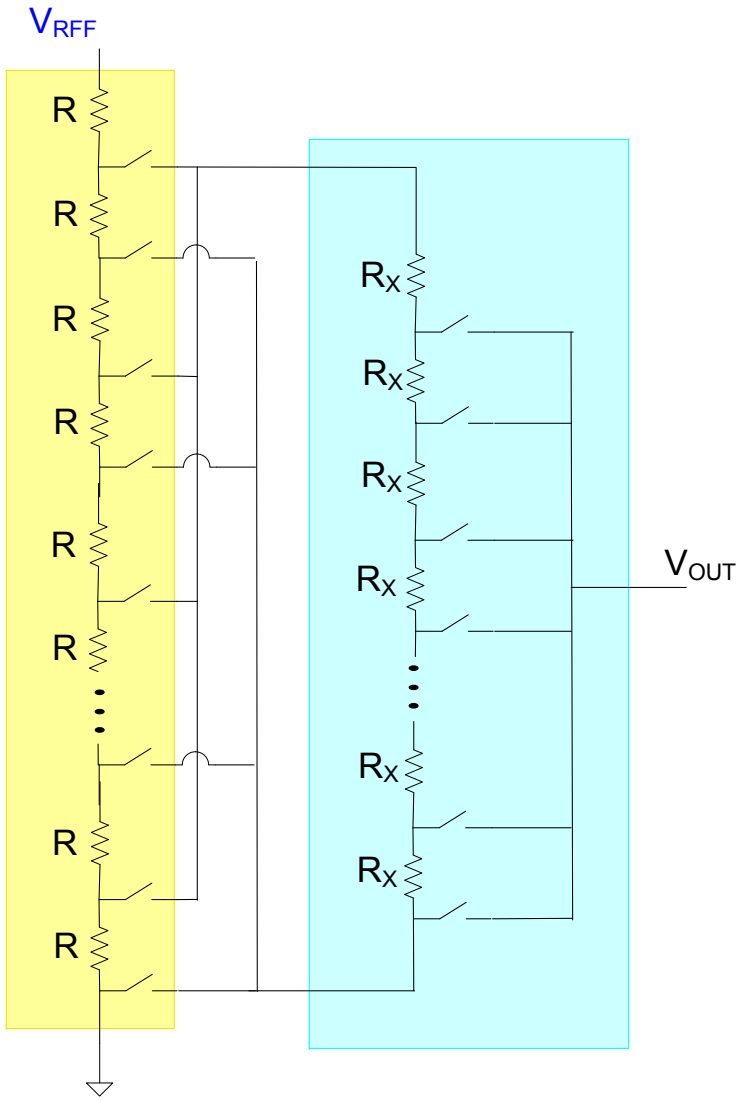
Types of DACs

R-string DAC



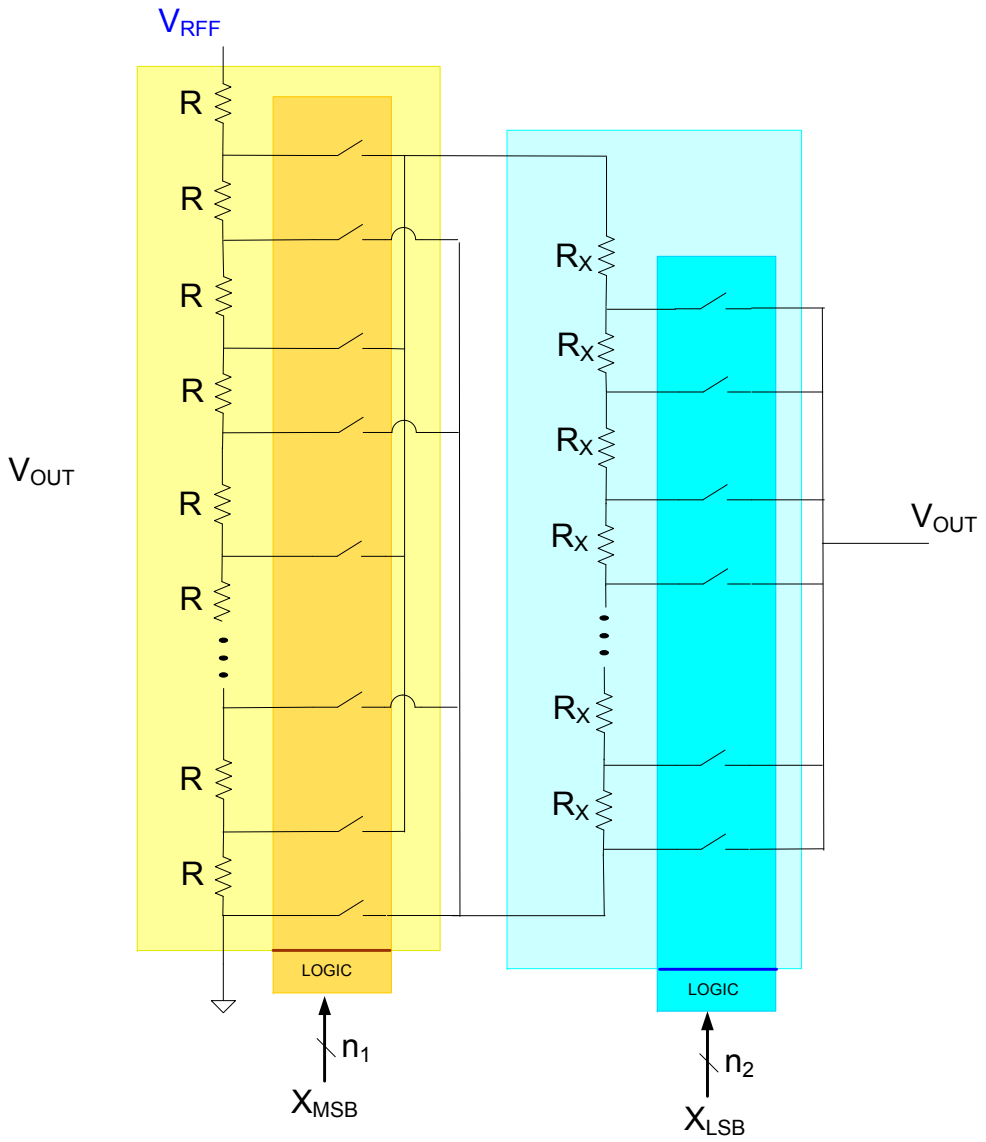
Types of DACs

Interpolating DAC



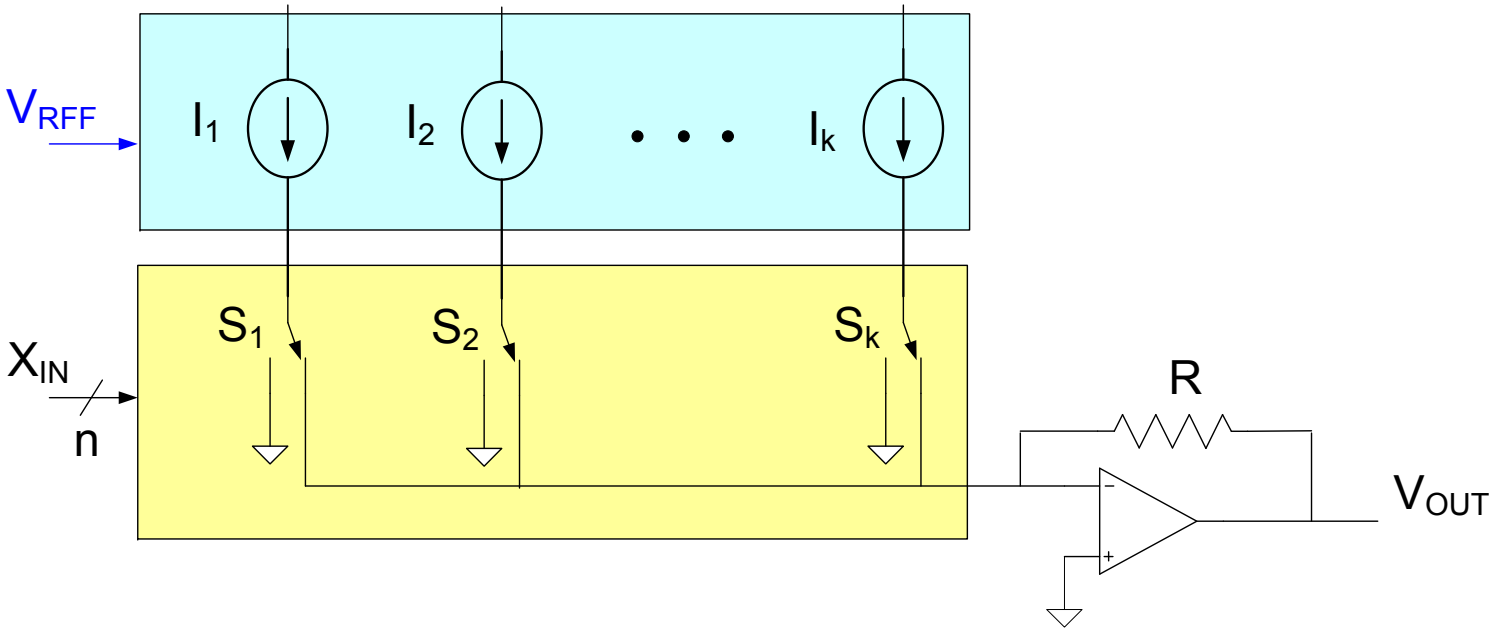
Types of DACs

Interpolating DAC



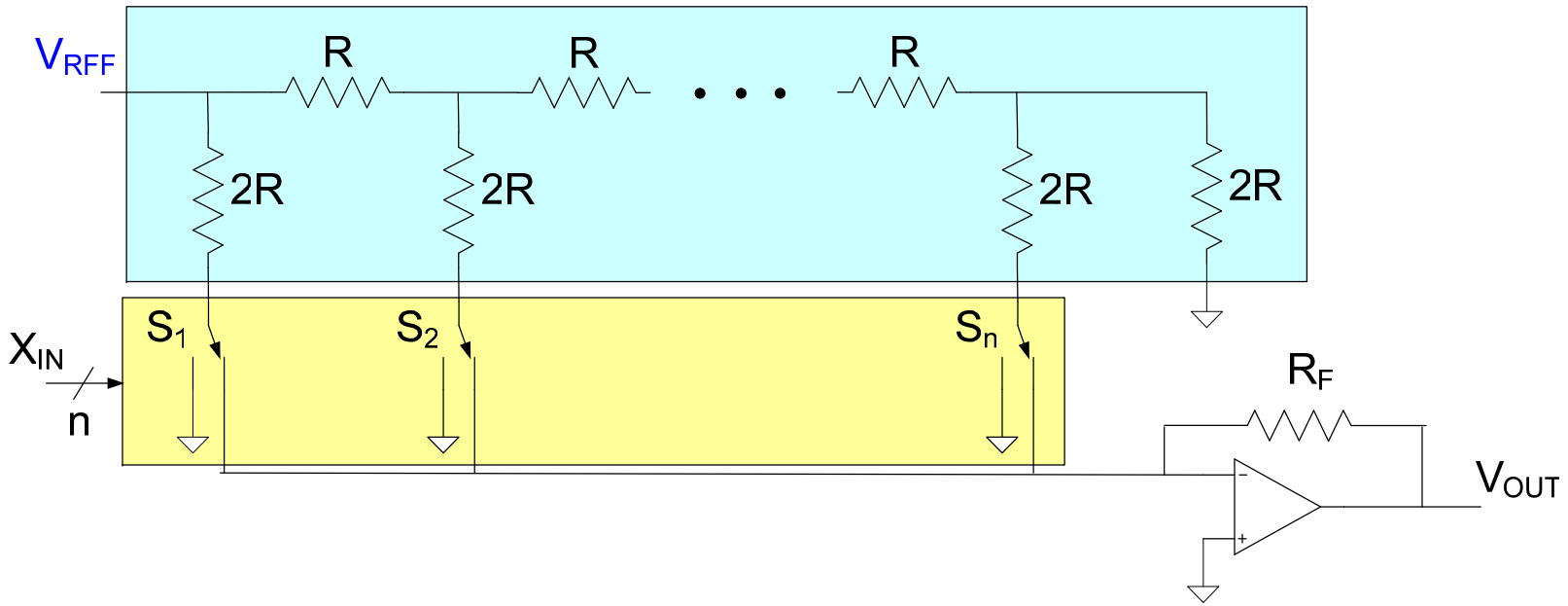
Types of DACs

Current-steering DAC



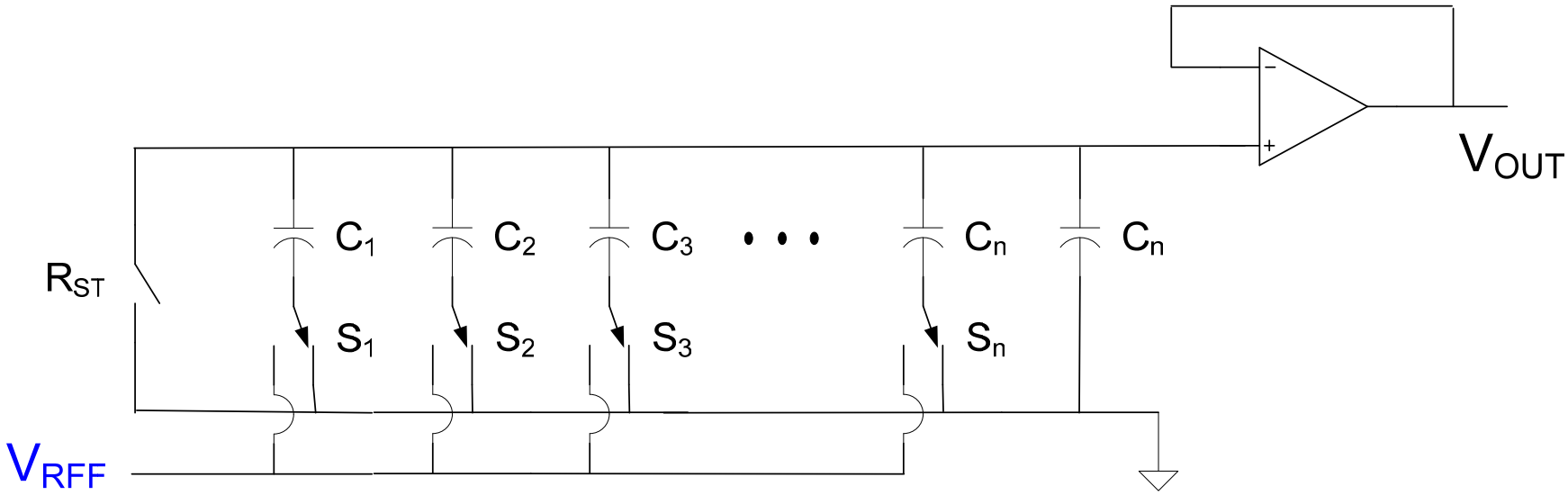
Types of DACs

Ladder DAC (R-2R)



Types of DACs

Charge-Redistribution DAC

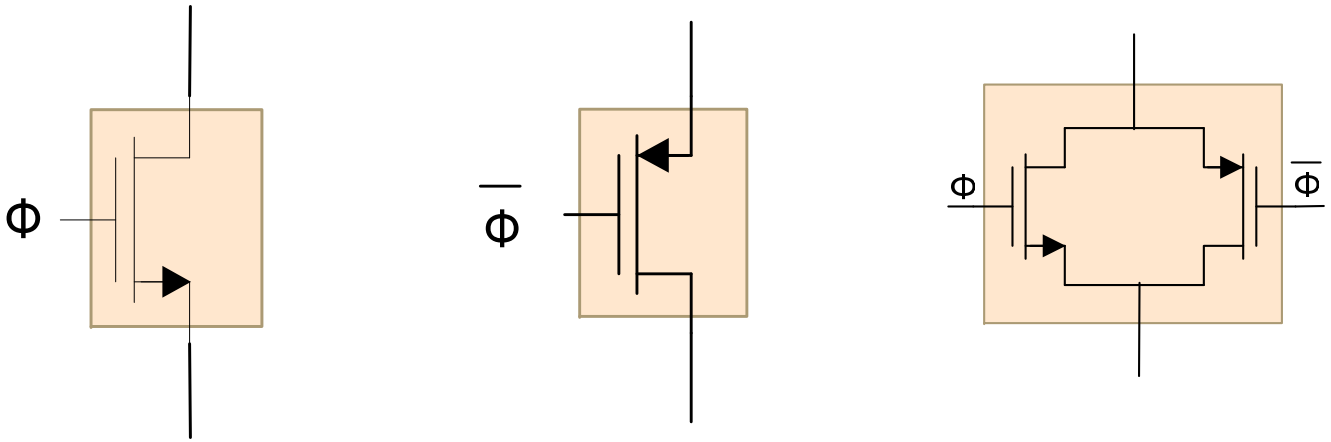


$$C_k = \frac{C}{2^{k-1}}$$

Observation: Most of the ADCs and DACs use switches

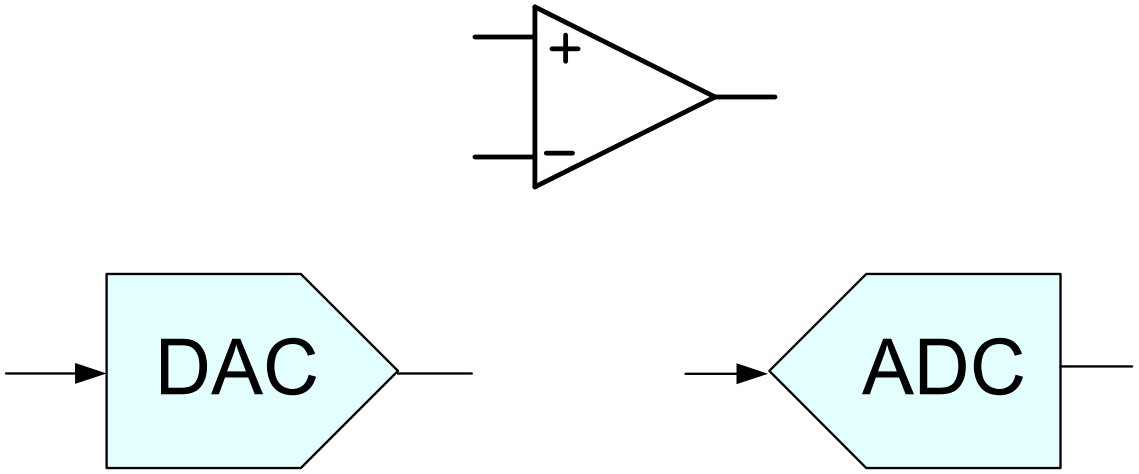
Switches used in DACs and ADCs DAC

Usually switches are simple a single MOS transistor or two MOS transistors



Engineering Issues for Using Data Converters

Much like with an op amp, it is essential that the engineer be familiar with the nonideal characteristics of a data converter to effectively use it



Much like an op amp, the engineer need not know much detail about the internal operations of the data converter to use them effectively

Engineering Issues for Using Data Converters

1. Inherent with Data Conversion Process

- Amplitude Quantization
- Time Quantization
- Present even with Ideal Data Converters

2. Nonideal Components

- Uneven steps
- Offsets
- Response Time
- Noise
- Present to some degree in all physical Data Converters

How do these issues ultimately impact performance ?

Engineering Issues for Using Data Converters

Inherent with Data Conversion Process

→ Time Quantization

- Amplitude Quantization

How do these issues ultimately impact performance ?

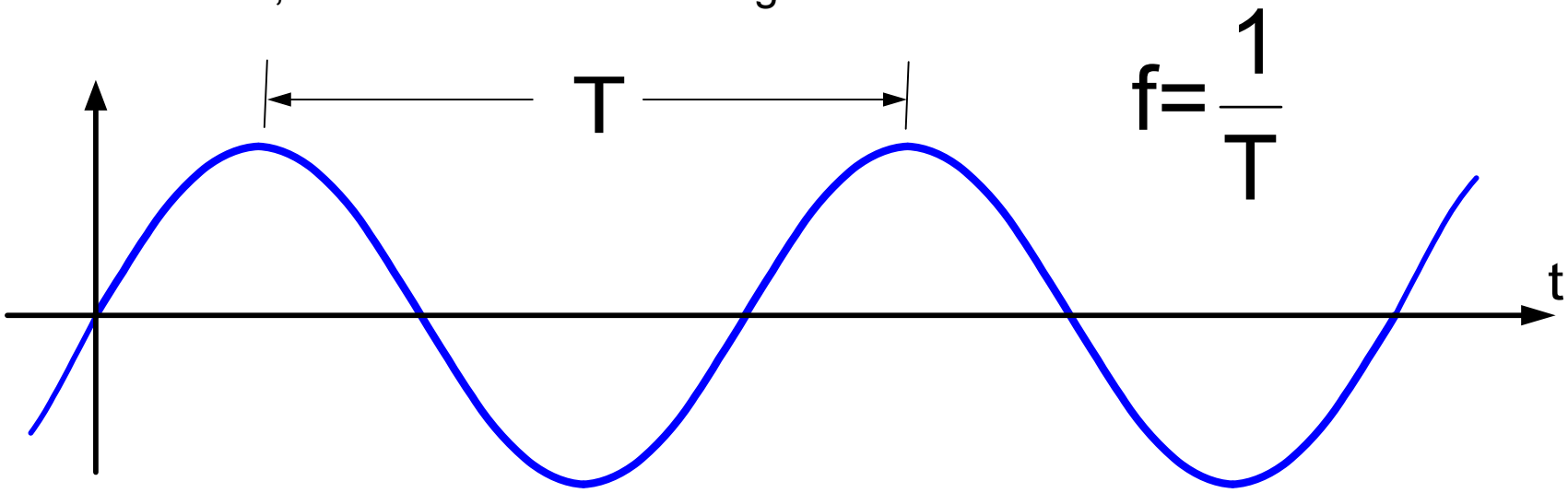
Time Quantization

Sampling Theorem

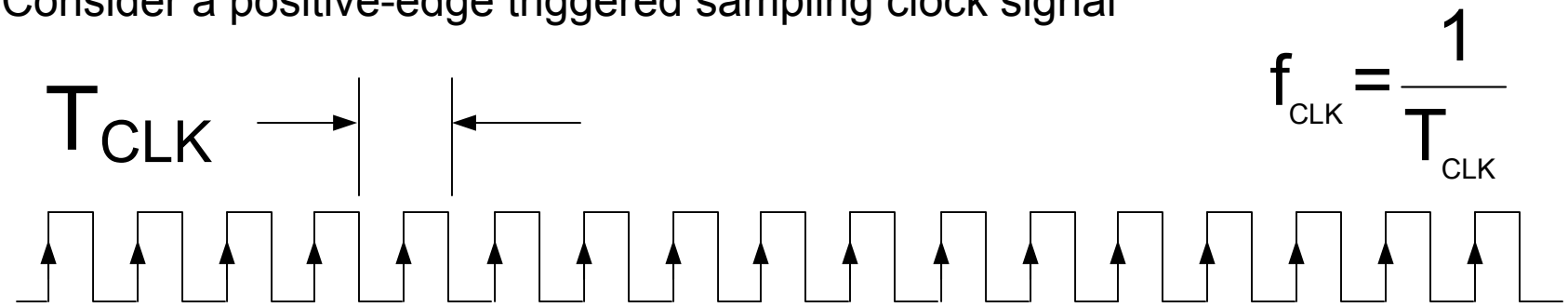
- Aliasing
- Anti-aliasing Filters
- Analog Signal Reconstruction

Time Quantization

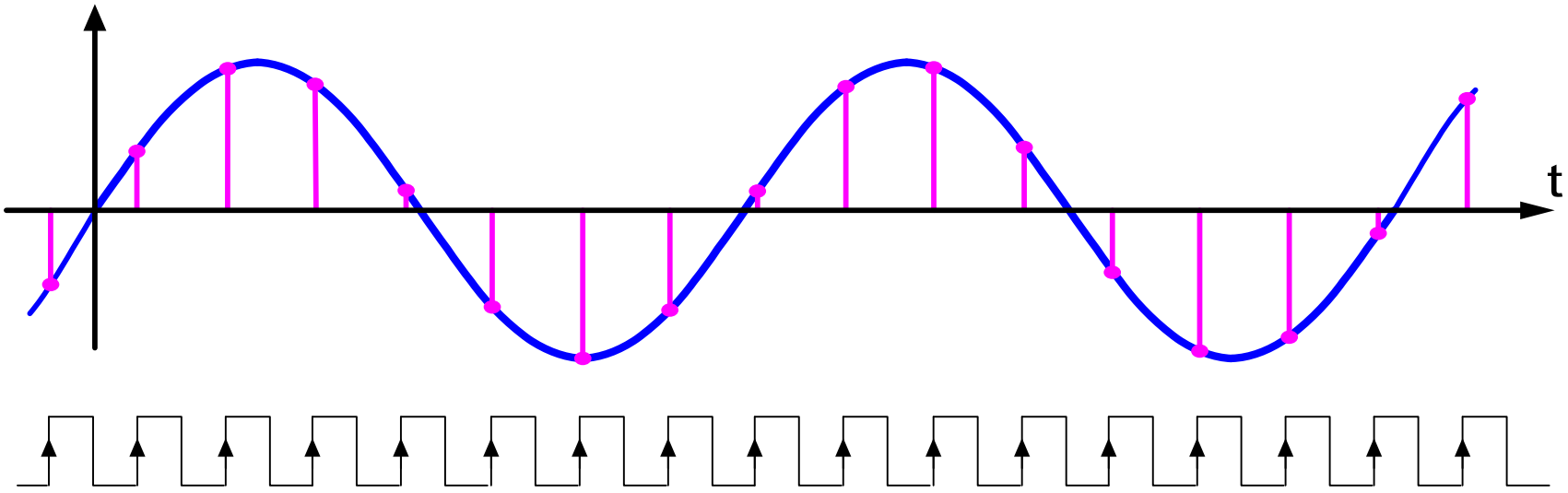
For convenience, consider a sinusoidal signal



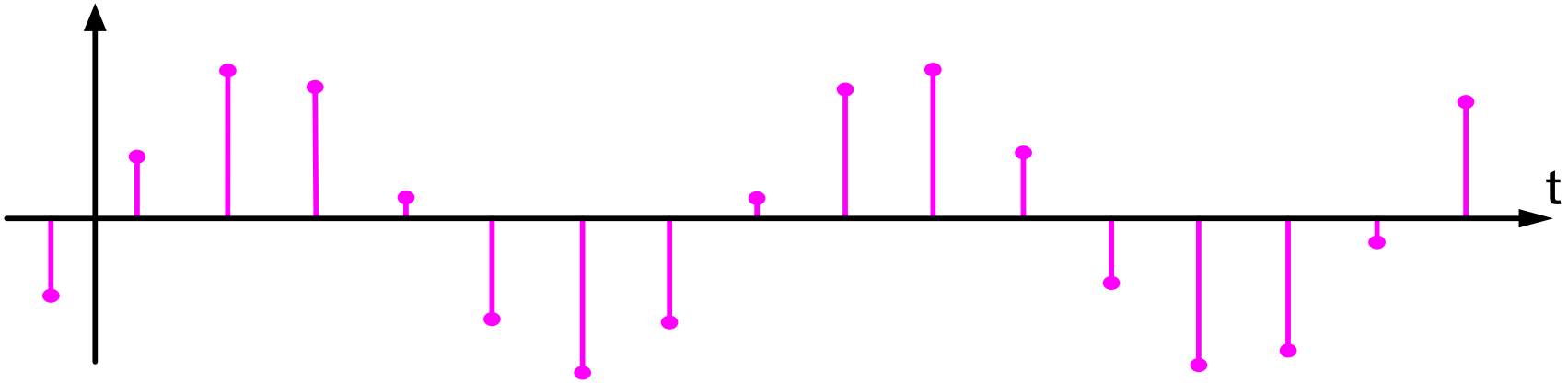
Consider a positive-edge triggered sampling clock signal



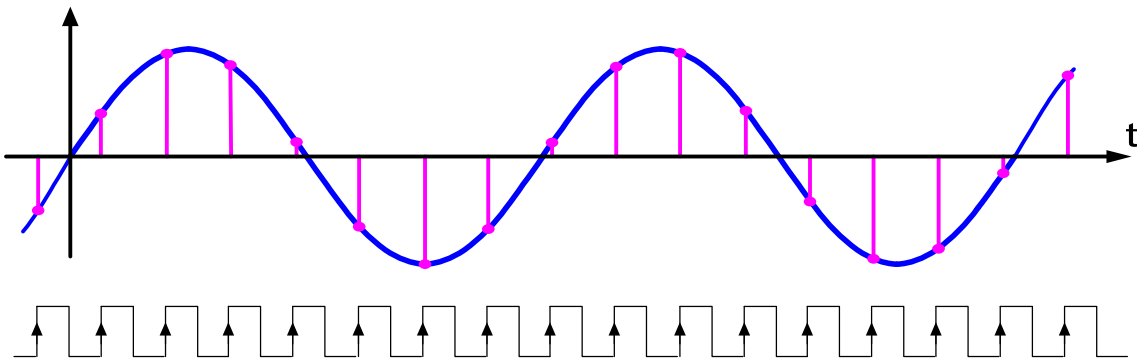
Time Quantization



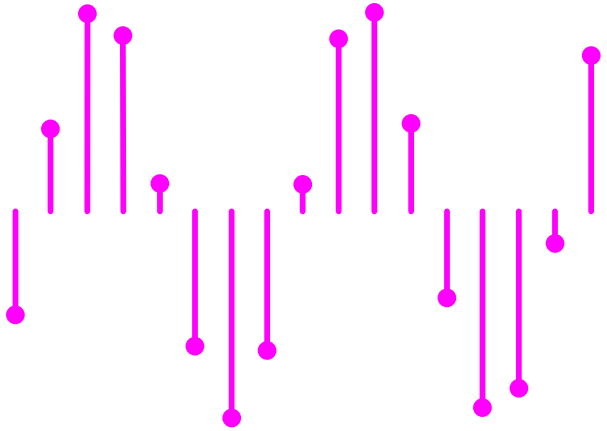
Time-quantized samples of signal



Time Quantization



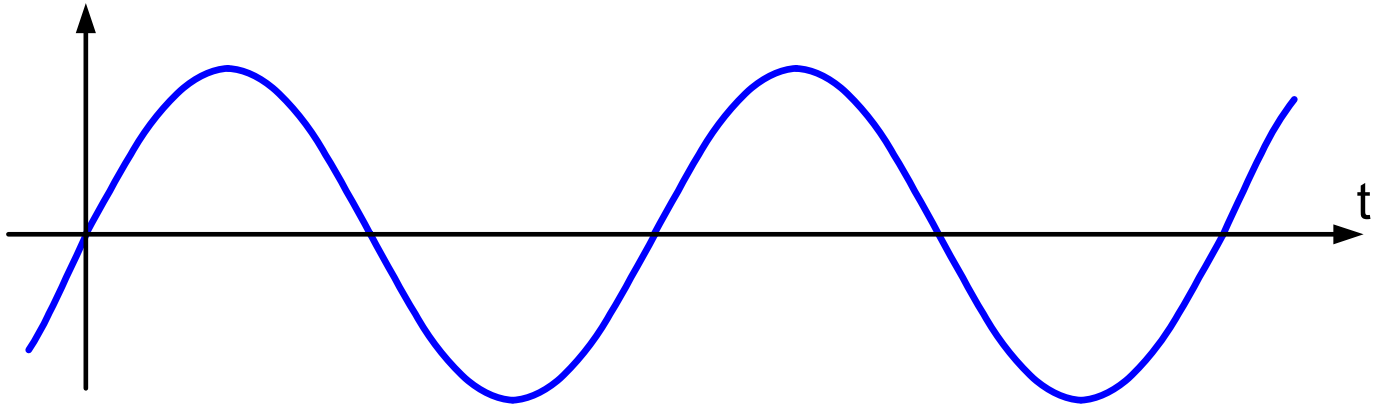
Time-quantized samples of signal



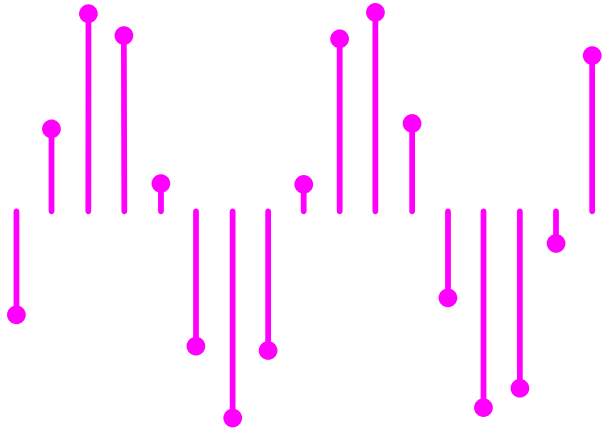
$[V_1, V_2, \ldots\ldots V_m]$

Once time-quantized, the samples become a sequence of real numbers and the time axis need no longer be specified (the time where the first sample was taken and the clock period may be recorded as real numbers as well)

Time Quantization

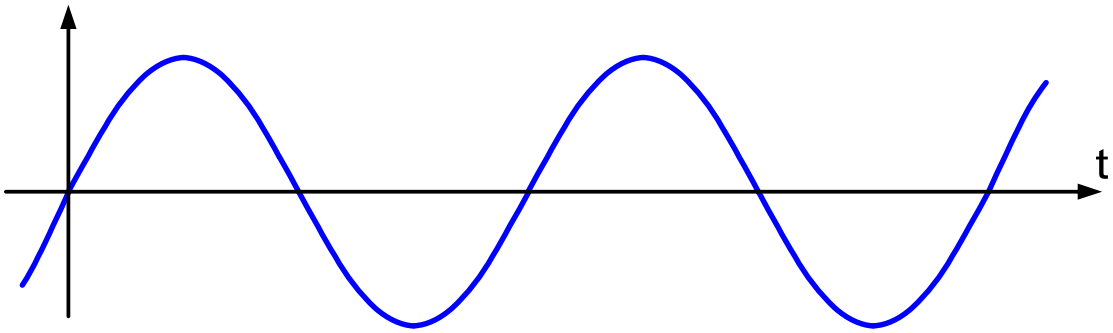


Time-quantized samples of signal

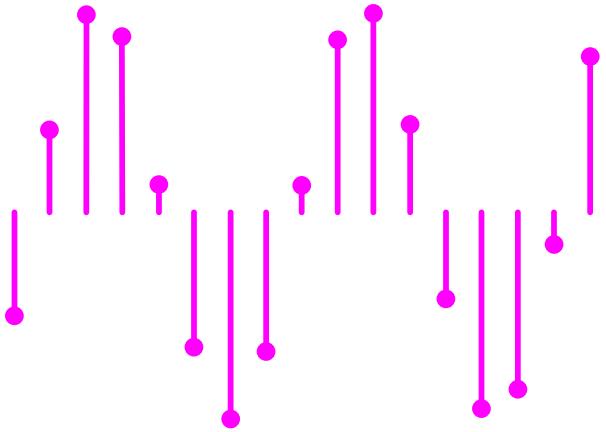


All information about original signal between the sample points is lost when the signal is sampled

Time Quantization



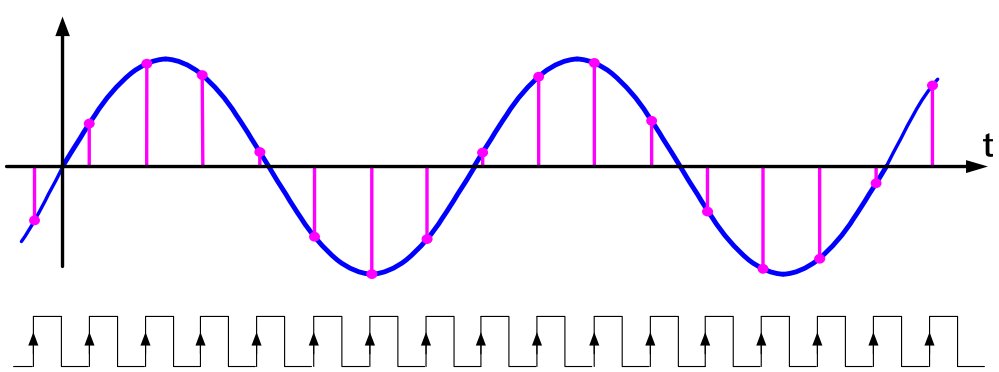
Time-quantized samples of signal

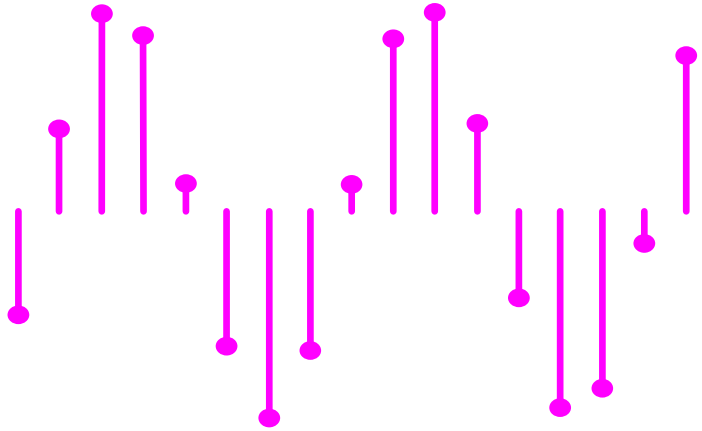


All information about original signal between the sample points is lost when the signal is sampled

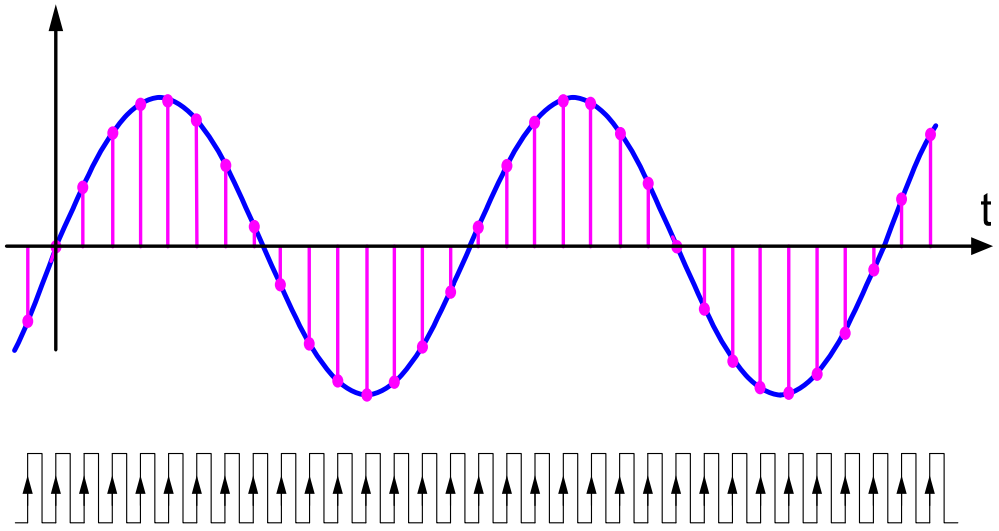
How often must a signal be sampled so that enough information about the original signal is available in the samples so that the samples can be used to represent the original signal ?

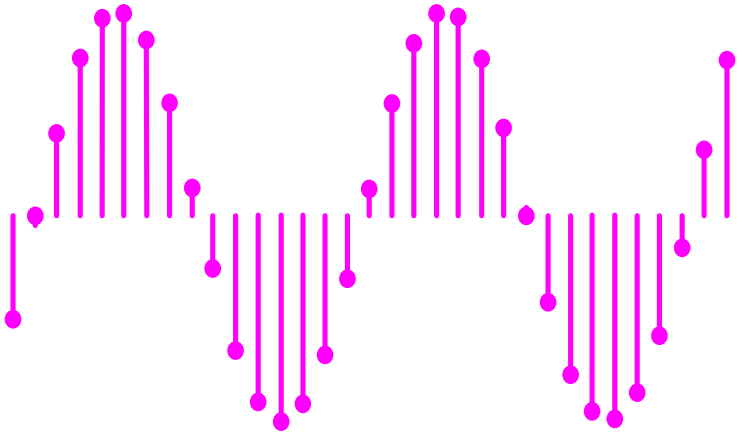
Time Quantization



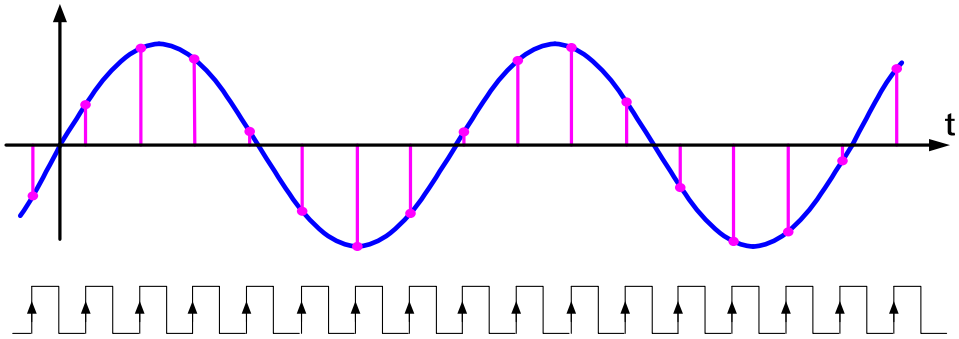


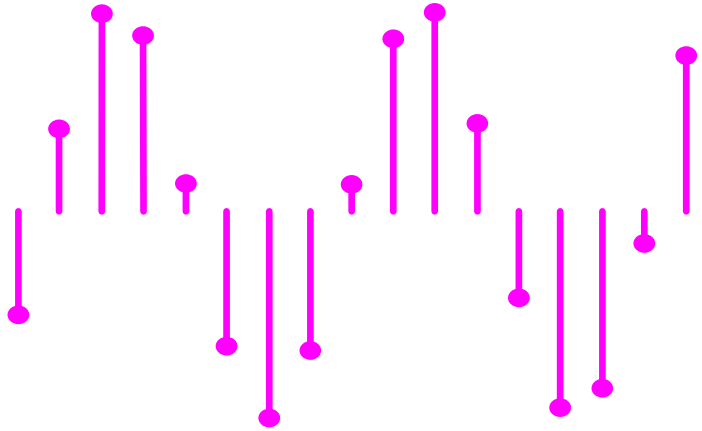
more samples:



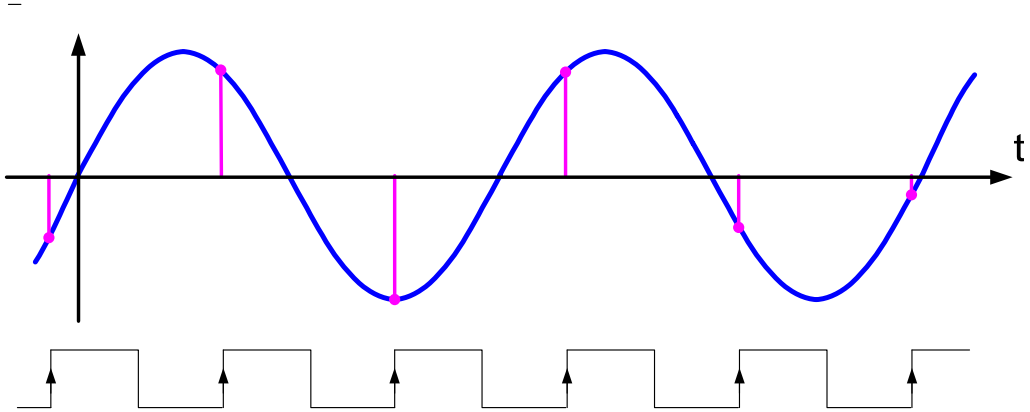


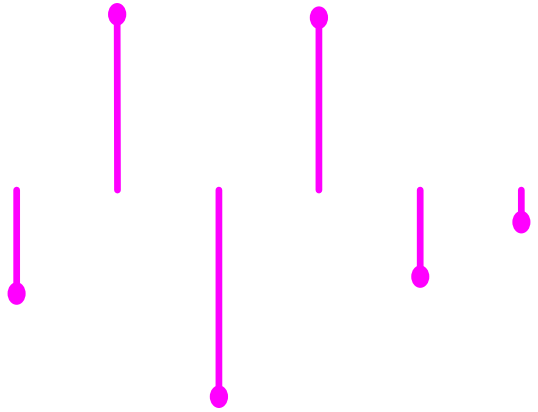
Time Quantization



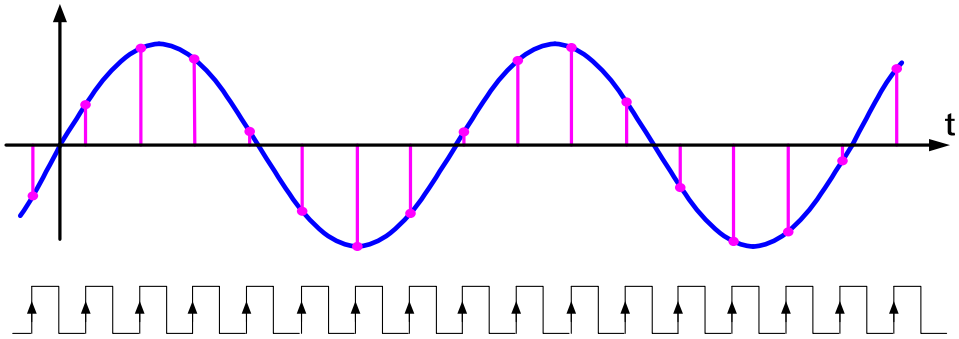


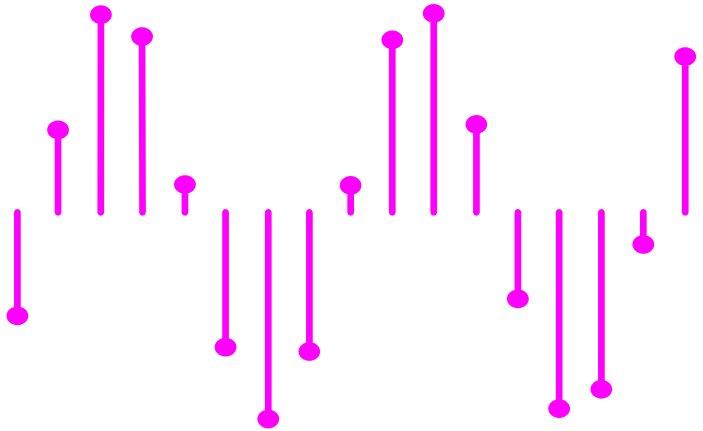
less samples:



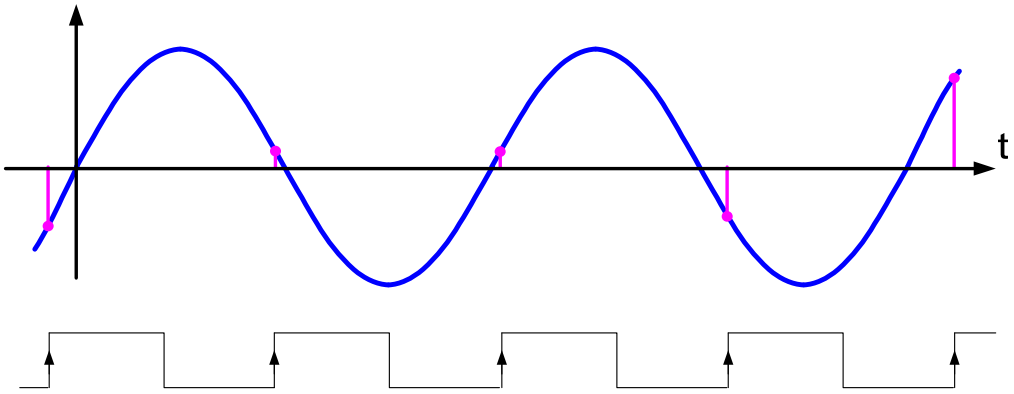


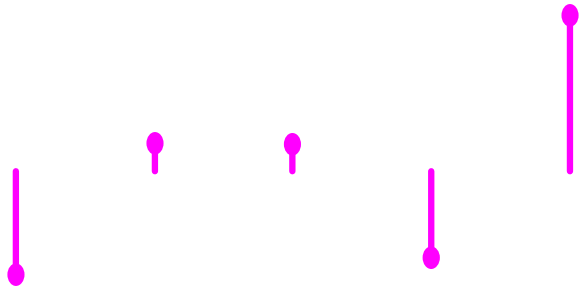
Time Quantization



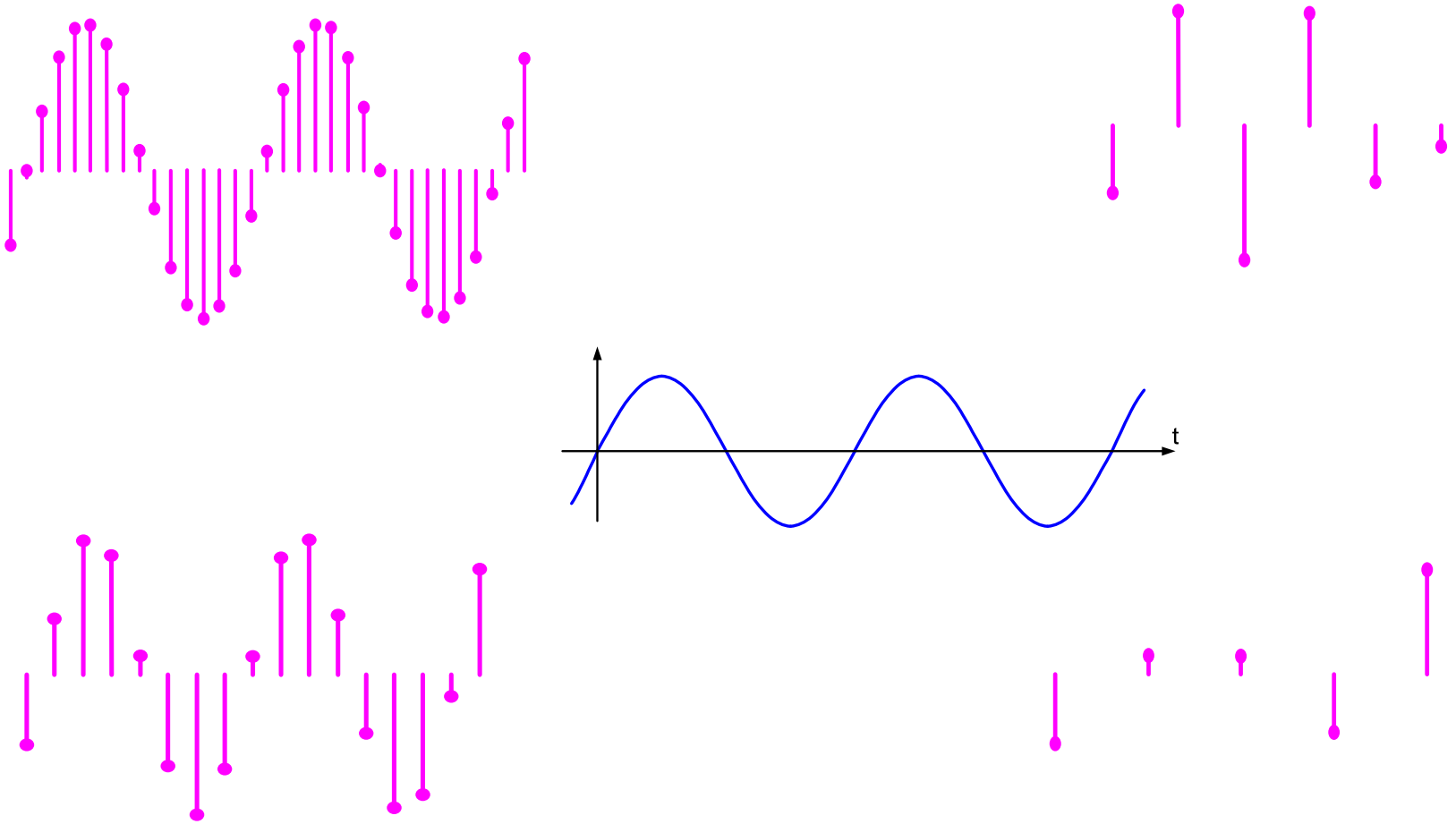


even less samples:



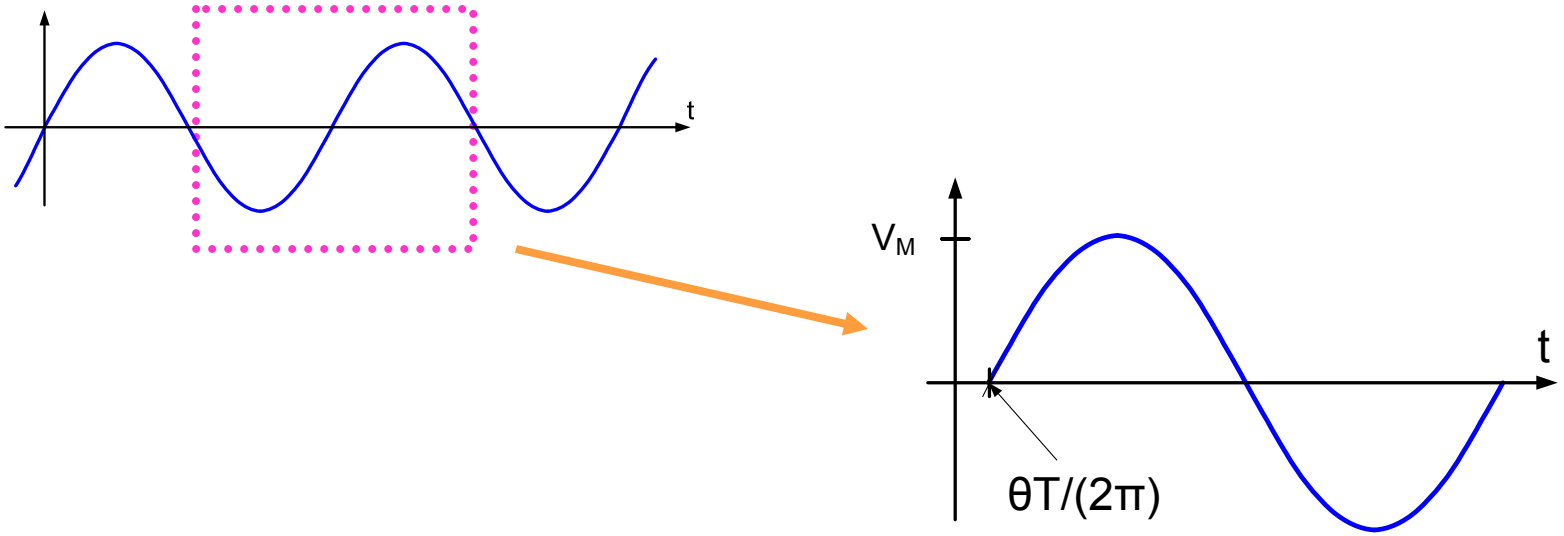


Time Quantization



How often must a signal be sampled so that enough information about the original signal is available in the samples so that the samples can be used to represent the original signal ?

Time Quantization



How often must a signal be sampled so that enough information about the original signal is available in the samples so that the samples can be used to represent the original signal ?

$$f(t)=V_M \sin(\omega t-\theta)$$

If the sampling times are known, there are two unknowns in this equation, V_M and θθ.

So two samples during this period that provide two non-zero values of f(t) will provide sufficient information to completely recreate the signal f(t)!

End of Lecture 37